Docket No.: V0195.0003
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Ralf Brederlow

Application No.: 10/714,536 Confirmation No.: 2199

Filed: November 13, 2003 Art Unit: 2813

For: POLYMER TRANSISTOR ARRANGEMENT, INTEGRATED CIRCUIT ARRANGEMENT AND METHOD FOR PRODUCING A POLYMER TRANSISTOR ARRANGEMENT

Examiner: C. E. Rodgers

AMENDED APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on September 21, 2006, and is in furtherance of said Notice of Appeal.

No fee is believed to be due for this Appeal Brief. Should any fees be required, please charge such fees to Deposit Account No. 50-2215.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. Real Party In Interest
II Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Claimed Subject Matter
VI. Grounds of Rejection to be Reviewed on Appeal
VII. Argument
VIII. Claims
IX. Evidence
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Evidence Appendix
Related Proceedings Appendix

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Infineon Technologies AG

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 12 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 1-12

2. Claims withdrawn from consideration but not canceled: None

3. Claims pending: 13-24

4. Claims allowed: None

5. Claims rejected: 13-24

C. Claims On Appeal

The claims on appeal are claims 13-24

IV. STATUS OF AMENDMENTS

Appellant filed an Amendment After Final Rejection on July 26, 2006. The Examiner responded to the Amendment After Final Rejection in an Advisory Action mailed August 8, 2006. In the Advisory Action, the Examiner indicated that Appellants' proposed amendments to claims 13-19 and 24 would not be entered.

Accordingly, the claims enclosed herein as Appendix A do not incorporate the amendments to claims 13-19 and 24 as indicated in the paper filed. However, the claims in Appendix A do incorporate the amendments indicated in the paper filed by Appellant on April 9, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 13 is directed to a polymer transistor arrangement *(100)* comprising: *[See Figs. 1, 8, and 9, and page 9, lines 9-10, page 18, lines 3-5, and page 19, lines 17-22, of the revised specification.]*

a polymer transistor formed in and/or on a substrate *(101)* including: *[See Figs. 1, 8, and 9, and page 9, lines 11-12, page 10, lines 9-13, and page 18, lines 6-7, of the revised specification.]*

a first source/drain region *(102)*; *[See Figs. 1, 8, and 9, and page 9, lines 17-18, page 18, lines 7-8 and 18-19, and page 19, lines 12-13, of the revised specification.]*

a second source/drain region *(103)*; *[See Figs. 1, 8, and 9, and page 9, lines 19-20, page 18, lines 12-14 and 17-18, and page 19, lines 15-16, of the revised specification.]*

a channel region *(104)* between the first and second source/drain regions; *[See Figs. 1, 8, and 9, and page 9, lines 20-24, page 18, lines 9-12, and page 19, lines 13-15, of the revised specification.]*

a gate region *(106)*; and *[See Figs. 1, 8, and 9, and page 9, lines 12-13, page 18, line 7, and page 19, lines 11-12, of the revised specification.]*

a gate-insulating layer *(105)* between the channel region and a gate region; and *[See Figs. 1, 8, and 9, and page 9, lines 13-17, page 10, line 6-9, page 18, line 9, and page 19, lines 11-12, of the revised specification.]*

a drive circuit *(107)* providing the first source/drain region with a voltage of sufficiently large magnitude and the gate region with a drain voltage of a sufficiently small magnitude, such that the polymer transistor has properties similar or identical to those of a Schottky diode. *[See Figs. 1, 8, and 9, and page 9, line 25, through page 10, line 5, of the revised specification.]*

Independent claim 24 is directed to a method for producing a polymer transistor arrangement *(100)*, comprising the steps of: *[See Figs. 1, 8, and 9, and page 9, lines 9-10, page 18, lines 3-5, and page 19, lines 17-22, of the revised specification.]*

forming a polymer transistor in and/or on a substrate *(101)* by: *[See Figs. 1, 8, and 9, and page 9, lines 11-12, page 10, lines 9-13, and page 18, lines 6-7, of the revised specification.]*

forming a first source/drain region *(102)*; *[See Figs. 1, 8, and 9, and page 9, lines 17-18, page 18, lines 7-8 and 18-19, and page 19, lines 12-13, of the revised specification.]*

forming a second source/drain region *(103)*; *[See Figs. 1, 8, and 9, and page 9, lines 19-20, page 18, lines 12-14 and 17-18, and page 19, line 15-16, of the revised specification.]*

forming a channel region *(104)* between the first and second source/drain regions; *[See Figs. 1, 8, and 9, and page 9, lines 20-24, page 18; lines 9-12, and page 19, lines 13-15, of the revised specification.]*

forming a gate region *(106)*; and *[See Figs. 1, 8, and 9, and page 9, lines 12-13, page 18, line 7, and page 19, lines 11-12, of the revised specification.]*

forming a gate-insulating layer *(105)* between the channel region and the gate region; and *[See Figs. 1, 8, and 9, and page 9, lines 13-17, page 10, lines 6-9, page 18, line 9, and page 19, lines 11-12, of the revised specification.]*

forming a drive circuit *(107)* that provides the first source/drain region with a voltage of sufficiently large magnitude and the gate region with a drain voltage of a

sufficiently small magnitude, such that the polymer transistor has properties similar or identical to those of a Schottky diode. *[See Figs. 1, 8, and 9, and page 9, line 25, through page 10, line 5, of the revised specification.]*

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 13-17 and 19-24 are unpatentable under 35 U.S.C. 103(a) over Bao et al. (US 6,150,668).

B. Whether claims 13-24 are unpatentable under 35 U.S.C. 103(a) over Jackson et al. (US 6,720,572).

VII. ARGUMENT

A. Rejection under 35 U.S.C. 103(a) over Bao et al. (US 6,150,668)

1. Claims 13-17 and 19-24

Claim 13 (similarly claim 24) recites, inter alia:

> A polymer transistor arrangement, comprising:
>
> ***a polymer transistor*** ...
>
> ***a drive circuit*** providing the first source/drain region with a voltage of sufficiently large magnitude and the gate region with a drain voltage of a sufficiently small magnitude such that the polymer transistor has properties similar or identical to those of a Schottky diode.

(Emphasis added.)

On page 3 and 5 of the Office Action, the Examiner states the following:

> Bao et al [Jackson et al.] does not specifically mention providing voltages such that the polymer transistor has properties similar or

> identical to those of a Schottky diode. However, this is merely an intended use of the structure as taught by Bao et al. [Jackson et al.]. It has been held that a claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). It would have been obvious to one of ordinary skill in the art at the time of invention to apply external stimuli such as voltages in any manner as best befits the application for which the structure is intended.

(Emphasis added.)

The Examiner is correct, as discussed in MPEP 2114 (E8R3), in that the manner of operating the device does not, by itself, differentiate an apparatus claim from the prior art. The relevant passage (the only location in the MPEP citing *Ex parte Masham*) states the following:

> A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987) (The preamble of claim 1 recited that the apparatus was "for mixing flowing developer material" and the body of the claim recited "means for mixing ..., said mixing means being stationary and completely submerged in the developer material." The claim was rejected over a reference which ***taught all the structural limitations*** of the claim ***for the intended use*** of mixing flowing developer. However, the mixer was only partially submerged in the developer material. The Board held that the ***amount of submersion is immaterial to the structure*** of the mixer and thus the claim was properly rejected.).

(Emphasis and underlining added.)

However, *Ex parte Masham* is not applicable to the present situation. The limitation of "a drive circuit providing the first source/drain region with a voltage of sufficiently large magnitude and the gate region with a drain voltage of a sufficiently small magnitude such that the polymer transistor has properties similar or identical to those of a Schottky diode" is not a statement of intended use, but is instead a functional limitation. MPEP 2173.05(g) states that "A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used." Therefore the "drive circuit ..." limitation should be accorded patentable weight.

The only reference to a drive circuit in Bao et al. is in the last sentence of the description: "Systems with the device of the present invention will also include appropriate drive circuitry." (This passage was also cited by the Examiner.).

Consequently, Bao et al. does not disclose (or suggest) a drive circuit set up to provide the first source/drain region with a voltage of sufficiently large magnitude and the gate region with a drain voltage of a sufficiently small magnitude, such that the polymer transistor has properties similar or identical to those of a Schottky diode. Bao et al. does not disclose (or suggest) a drive circuit with the particular design and set up required of the transistor as a diode as recited in the claims.

Claims 13-17 and 19-24 are, therefore, patentable over Bao et al.

B. Rejection under 35 U.S.C. 103(a) over Jackson et al. (US 6,720,572)

1. Claims 13-24

Claim 13 (similarly claim 24) recites, inter alia:

A polymer transistor arrangement, comprising:

> ***a polymer transistor*** ...
>
> ***a drive circuit*** providing the first source/drain region with a voltage of sufficiently large magnitude and the gate region with a drain voltage of a sufficiently small magnitude such that the polymer transistor has properties similar or identical to those of a Schottky diode.

(Emphasis added.)

On page 3 and 5 of the Office Action, the Examiner states the following:

> Bao et al [Jackson et al.] does not specifically mention providing voltages such that the polymer transistor has properties similar or identical to those of a Schottky diode. However, this is merely an intended use of the structure as taught by Bao et al. [Jackson et al.]. It has been held that a claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). It would have been obvious to one of ordinary skill in the art at the time of invention to apply external stimuli such as voltages in any manner as best befits the application for which the structure is intended.

(Emphasis added.)

The Examiner is correct, as discussed in MPEP 2114 (E8R3), in that the manner of operating the device does not, by itself, differentiate an apparatus claim from the prior art. The relevant passage (the only location in the MPEP citing *Ex parte Masham*) states the following:

> A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the

> claim. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987) (The preamble of claim 1 recited that the apparatus was "for mixing flowing developer material" and the body of the claim recited "means for mixing ..., said mixing means being stationary and completely submerged in the developer material." The claim was rejected over a reference which ***taught all the structural limitations*** of the claim ***for the intended use*** of mixing flowing developer. However, the mixer was only partially submerged in the developer material. The Board held that the ***amount of submersion is immaterial to the structure*** of the mixer and thus the claim was properly rejected.).

(Emphasis and underlining added.)

However, *Ex parte Masham* is not applicable to the present situation. The limitation of "a drive circuit providing the first source/drain region with a voltage of sufficiently large magnitude and the gate region with a drain voltage of a sufficiently small magnitude such that the polymer transistor has properties similar or identical to those of a Schottky diode" is not a statement of intended use, but is instead a functional limitation. MPEP 2173.05(g) states that "A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used." Therefore the "drive circuit ..." limitation should be accorded patentable weight.

The passage of Jackson et al. cited by the Examiner for disclosing a drive circuit, states the following:

> A voltage applied between contacts 18 and 24 sets up an electric field in organic TFT layer 20 and organic LED layer 22. A voltage applied to gate electrode 14 controls this electric field. That is, the voltage on gate electrode 14 controls the brightness of light emitted by LED layer 22. Light emitting device 10 is useful as a pixel in a display.

Consequently, Jackson et al. does not disclose (or suggest) a drive circuit set up to provide the first source/drain region with a voltage of sufficiently large magnitude and the gate region with a drain voltage of a sufficiently small magnitude, such that the polymer transistor has properties similar or identical to those of a Schottky diode. Jackson et al. does not disclose (or suggest) a drive circuit with the particular design and set up required of the transistor as a diode as recited in the claims.

Claims 13-23 and 24 are, therefore, patentable over Jackson et al.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Claims Appendix. As indicated above, the claims in Claims Appendix do include the amendments filed by Appellant on April 9, 2006, and do not include the amendments filed on July 26, 2006.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above.

Dated: October 17, 2006

Respectfully submitted,

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CLAIMS APPENDIX

Claims Involved in the Appeal of Application Serial No. 10/714,536

13. A polymer transistor arrangement, comprising:

a polymer transistor formed in and/or on a substrate including:

a first source/drain region;

a second source/drain region;

a channel region between the first and second source/drain regions;

a gate region; and

a gate-insulating layer between the channel region and a gate region; and

a drive circuit providing the first source/drain region with a voltage of sufficiently large magnitude and the gate region with a drain voltage of a sufficiently small magnitude, such that the polymer transistor has properties similar or identical to those of a Schottky diode.

14. The polymer transistor arrangement as claimed in claim 13, wherein the drive circuit provides the source/drain regions and the gate region with electrical potentials such that the junction between one of the two source/drain regions and the channel region is connected as a reverse-biased diode.

15. The polymer transistor arrangement as claimed in claim 13, wherein the channel region and the source/drain regions are produced from a material such that the junction between one of the source/drain regions and the channel region is one of a Schottky junction, an in junction, an ip junction, and a pn junction.

16. The polymer transistor arrangement as claimed in claim 13, wherein the drive circuit provides electrical potentials such that a magnitude of the gate voltage is greater than a magnitude of the voltage between the source/drain regions.

17. The polymer transistor arrangement as claimed in claim 13, wherein the junctions between respective ones of the source/drain regions and the channel region are formed geometrically asymmetrically with respect to one another.

18. The polymer transistor arrangement as claimed claim 13, wherein one of the source/drain regions is formed at least partially on the channel region and the other source/drain region is formed at least partially below the channel region.

19. An integrated circuit arrangement having the polymer transistor arrangement as claimed in claim 13.

20. The integrated circuit arrangement as claimed in claim 19, wherein the integrated circuit arrangement is a reference voltage circuit.

21. The integrated circuit arrangement as claimed in claim 19, wherein the integrated circuit arrangement is a temperature-compensated reference voltage circuit.

22. The integrated circuit arrangement as claimed in claim 19, wherein the integrated circuit arrangement is a current source.

23. The integrated circuit arrangement as claimed in claim 19, wherein the integrated circuit arrangement is a voltage control circuit.

24. A method for producing a polymer transistor arrangement, comprising the steps of:

forming a polymer transistor in and/or on a substrate by:

forming a first source/drain region;

forming a second source/drain region;

forming a channel region between the first and second source/drain regions;

forming a gate region; and

forming a gate-insulating layer between the channel region and the gate region; and

forming a drive circuit that provides the first source/drain region with a voltage of sufficiently large magnitude and the gate region with a drain voltage of a sufficiently small magnitude, such that the polymer transistor has properties similar or identical to those of a Schottky diode.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.